REMARKS

In accordance with the foregoing, the specification and claims 1-7 have been amended. No new matter is presented and, accordingly, approval and entry of the foregoing amendments are respectfully requested.

STATUS OF CLAIMS

Claims 1-5 are rejected.

Claims 6-8 are objected to.

Claims 1-8 are pending and under consideration.

AT PAGE 2 OF THE ACTION: OBJECTIONS TO THE DRAWINGS

In accordance with the foregoing, replacement drawings of FIGS. 1-5, designating same by the legend - -PRIOR ART- -, are herewith submitted.

AT PAGE 2 OF THE ACTION: OBJECTIONS TO CLAIMS 1 THROUGH 8

Claims 1-8 have been amended, adopting the Examiner's suggested changes to overcome the objections.

AT PAGE 3 OF THE ACTION: REJECTION OF CLAIM 4 UNDER 35 U.S.C. §102(a) FOR ANTICIPATION BY ADMITTED PRIOR ART (AAPA);

AT PAGE 4 OF THE ACTION: REJECTION OF CLAIMS 1-3 UNDER 35 U.S.C. §103(a) FOR ANTICIPATION BY ADMITTED PRIOR ART (AAPA) IN VIEW OF SODA (U.S. PATENT 5,956,378);

AT PAGE 5 OF THE ACTION: REJECTION OF CLAIM 5 UNDER 35 U.S.C. §103(a) FOR ANTICIPATION BY ADMITTED PRIOR ART (AAPA) IN VIEW OF BLUM (U.S. PATENT 5,757,218)

The rejections are respectfully traversed.

At page 4 of the Action, in the rejection of claim 1, the Examiner first relies on AAPA as disclosing "a timing extraction circuit which uses a PLL circuit containing a phase comparative circuit..." but then concedes that:

> AAPA does not disclose the timing extraction circuit further comprise a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for

> controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization.

(Action at page 4)

The Examiner then attempts to overcome the admitted deficiency of the AAPA by contending that "in analogous art, Soda teaches a PLL circuit comprising a detection circuit for detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of prescribed pattern; and a control circuit for controlling upon detecting said absence, the phase of said clock signal in order to maintain synchronization (see FIG. 2, component 23 and col. 4, lines 14-33)."

However, it is respectfully submitted that the Examiner errs in his interpretation of the disclosure of Soda. Particularly, Soda merely discloses a detection circuit for detecting a collapse of synchronization and a PLL circuit having a control circuit for controlling, in response to the detection of the collapse of synchronization, the oscillation frequency of a VCO - -and, thus, discloses no circuit for maintaining synchronization, as in the present invention.

Moreover, claim 1 recites, in the first paragraph of the body of the claim:

> a detection circuit detecting the absence of an output of phase comparison information from said phase comparator circuit by receiving a data signal of a prescribed pattern.

This "detection circuit..." recited in claim 1 is a novel component of the claimed timing extraction circuit of claim 1 and is distinctive and neither disclosed nor suggested by Soda.

Further, although the Examiner contends at page 5, lines 1-3, that "Soda further teaches control circuit controls the phase of said clock signal by inverting said clock signal (see col. 6, lines 15-39)", Soda, in actuality, merely shows a circuit for controlling the number of inverter circuits for changing the frequency range of a ring oscillator composed of a combination of the inverter circuits. Thus, Soda discloses no means for inverting phase without changing a frequency.

Accordingly, claims 1-3 patentably distinguish over Soda.

Re claim 4

In operation of the circuit shown in FIG. 3 of the present application (AAPA), when the input data pattern and the phase relationship between the input data and the clock signal become as illustrated in FIG. 7, signal changes from 0 to 1 and 1 to 0 occur, even though the input data has phase information. Therefore, the circuit of the AAPA cannot detect a phase

difference relative to the clock signal, which is one of the problems solved by the present invention.

The invention, as defined by each of claims 1-4, then solves the above problems caused by the circuit of the AAPA..

Re claim 5

In the rejection of claim 5 on page 5, line 6 et. seq. of the Action, the Examiner concedes that:

> AAPA does not disclose a duty cycle evaluation circuit and a controlled circuit controlling the signal in response to the duty cycle evaluation circuit.

(Action at page 5)

The Action then seeks to overcome the admitted deficiency of AAPA by contending that:

> However, in analogous art, Blum teaches a duty cycle evaluation circuit for evaluating a duty cycle between input data before and after a point which said PLL circuit is locked (see FIG. 1, component 14), and a control circuit for controlling, based on a result of said evaluation, a data discrimination phase before and after the point at which said PLL circuit is locked (see FIG. 1, component 106).

(Action at page 5, lines 11-12)

However, Blum merely discloses a circuit for detecting a duty cycle of a clock signal - - and, after the detection, correcting the duty cycle.

The invention of claim 5 does not define a circuit for correction of clock duty cycle, as in Blum, but a circuit evaluating a duty cycle with an appropriate phase with respect to a data signal having a duty cycle deviation at every other one bit, as shown by (A) in FIG. 23(a) - - a clear distinction over Blum.

Accordingly, it is respectfully submitted that claims 1-5 patentably distinguish over the references and rejections of record.

ALLOWABLE SUBJECT MATTER

Claims 6-8 are objected to but are indicated to be allowable if suitably rewritten to be dependent upon a rejected base claim or if rewritten to independent form including all the limitations of the respective base and any intervening claims. The indication of allowable subject matter as to claims 6-8 is greatly appreciated; however, those claims are not being rewritten to independent form, as suggested by the Examiner, in view of the foregoing demonstration of the patentability of claims 1-5.

CONCLUSION

It is respectfully submitted that the foregoing has clearly distinguished the pending claims over the references and rejections of record. Further, all outstanding objections have been overcome by the foregoing. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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